

Satyanarayana kamparaju

Firmware Developer

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PROFILE SUMMARY

- Detail-oriented and technically adept **Embedded systems Firmware Driver Developer** with 1+ years of hands-on experience in developing, and debugging embedded systems firmware for microcontroller-based and SoC platforms. Experienced in **firmware development**, including bootloader, driver, and protocol stack integration.
- Seeking challenging opportunities in Embedded Firmware Development where deep technical expertise and analytical skills can drive product innovation and quality.
- Currently Working with "ASSETON TECHNOLOGIES PRIVATE LIMITED" from "FEB 2024" till date.

PROFESSIONAL EXPERIENCE

- Proficiency in developing and testing Embedded Firmware on **8-Bit, and 32-Bit Microcontrollers**.
- Worked on Firmware driver development for critical modules like **IIC,UART**.
- Strong in **C, Embedded C** and aware of **Assembly Language**.
- Hands on experience on driver development for interfacing of **LED,Relay, 7 Segment Display and LCD**.
- Experience in Firmware testing methodology, including writing and execution of **test plans, debugging**.
- Worked closely with the Verification and Validation test group to resolve any coding **issues/bugs**.
- Responsible for the **analysis, Programming, debugging** and modification of firmware applications.
- Experience in use of advanced development/ debugging tools: **JTAG debuggers, oscilloscopes, and Logical Analyzers**.
- Involved on the **board bring up activities and bug tracking tools** such as **JIRA**.
- Expert in understanding of **Hardware Schematics** and **Hardware Fundamentals**.
- Having Good communication skills for collaborating with cross-functional teams.
- Expert in understanding **datasheets** and **manuals** for different **IP's and SOC's**.

TECHNICAL SKILLS

Programming Languages: C, Python, Embedded C

Protocols: UART, IIC, SPI, CAN, SDHC3.0.

Software Tools: STM32CubeIDE, Keil v5.0, Trace 32, GIT, GDB, GCC.

Hardware Tools: logical Analyzer, JTAG, Oscilloscope, Protocol Analyzer, DMM[Digital Multi Meter].

PROJECTS

Project 1: Clock & Power Management

- Designed and developed firmware modules for **SoC clock management**, including initialization of **PLLs, oscillators, clock dividers, and multiplexers** across CPU, memory, and peripheral domains.
- Implemented **clock tree bring-up routines** in early boot firmware, ensuring reliable startup of system and peripheral domains.
- Developed and validated **DFS (Dynamic Frequency Scaling)** and **DVFS (Dynamic Voltage and Frequency Scaling)** firmware routines to balance **performance and power efficiency**.
- Programmed **register-level clock controller configurations** (enable/disable, set rate, change parent source, gating) for CPU, memory, and other high-speed interfaces.
- Integrated **low-power clock management features**, enabling safe transitions between **sleep, standby, and active states** with minimal wake-up latency.
- Ensured **PLLs lock and stabilize** before subsystem transitions, improving **system stability and reliability**.
- Debugged and resolved **clock-related failures** (boot hangs, unstable PLLs, misconfiguration, synchronization glitches) using JTAG, oscilloscopes, and trace logs.
- Collaborated with **hardware and RTL design teams** to analyze and fix clock initialization issues observed in **pre-silicon and post-silicon validation**.

Project 2: Firmware Development SDHC3.0

Roles & Responsibilities:

- Developed and tested firmware for SDHC interface compliance per SD specifications.
- Implemented state machines for card initialization and command sequences.
- Wrote ISR (Interrupt Service Routines) to manage transfer completion, error handling, and event monitoring.

Features Development SDHC3.0:

- Card Detection and Hot-Swap.
- Power Management.
- Multi-block Read/Write Enhancements.
- Performance Optimization.
- Compatibility & Compliance.
- Error handling & recovery.

Project 3: Firmware Development for UART(16650) & IIC Master Controller

Roles & Responsibilities:

- Developed and executed **comprehensive test cases** to validate IIC and UART interfaces in both master and slave configurations.
- Verified protocol-level operations including **start/repeated start/stop conditions** for IIC and **framing, parity, and stop bits** for UART.
- Implemented data transmission and reception using **polling mechanism, interrupt, and DMA-based mechanisms** across both interfaces.
- Debugged communication issues and **boot failures** using tools like **JTAG, serial console logs, and oscilloscopes**.
- Validated **data integrity, synchronization, and timing compliance** across multiple data lengths and baud rates.
- Ensured **proper error handling and recovery mechanisms** for scenarios such as NACKs, overrun, underrun, and framing errors.
- Collaborated with hardware, design, and software teams to analyze and resolve interface-level issues.
- Used **JIRA** to log bugs, track progress, and support issue resolution throughout the development cycle.
- Conducted **regression and stress testing** to ensure stable performance of both IIC and UART modules under different system loads.

EDUCATION

B.Tech

Kalasalingam Academy of research and Education
Electronic Communication Engineering

Intermediate

NSR Impluse Junior College